March 27, 2012

C8051F52xA/F53xA and C8051F52x/F53x Errata

Errata Status Summary

This document summarizes all known errata with these devices.

Errata #	Title	Impact	'F52xA/53xA (Rev. B) 'F52x/53x (Rev. A)	'F52x-C/53x-C (Rev. C)
1	Oscillator Wakeup	Minor	Issue exists	Issue fixed
2	Cold Programming Temperature on industrial grade (-I) parts only.	Minor	Issue exists	Issue exists
3	Long-reset Oscillator Lockup	Minor	Issue resolved from date code "1124"	Issue fixed
4	VDD Monitor Low Threshold	Information	Issue exists	Issue exists

Impact Definition: Each erratum is marked with an impact, as defined below:

- Minor—Workaround exists.
- Major—Errata that do not conform to the data sheet or standard.
- Information—The device behavior is not ideal but acceptable. Typically, the data sheet will be changed to match the device behavior.

Errata Details

1. **Description**: When a device enters a low power suspend mode by setting the SUSPEND bit in OSCICN, there is a low probability of the device remaining in suspend even when a wake-up condition is triggered.

   Impact: The device remains in suspend mode until a power-on reset.

   Workaround: To prevent the issue, set the ZTCEN bit in REF0CN to 1 before entering suspend mode. This will slightly increase the supply current in suspend mode but it will prevent the issue.

   Resolution: Revision C of the device will not require setting ZTCEN before entering suspend mode.

2. **Description**: For –I (Industrial Grade) parts, a cold temperature programming deficiency may be present on weak flash memory bits. There is no problem programming the flash at 0 °C and above. There is

only a potential flash read issue if programming was done at cold temperature below 0 °C. If programmed at 0 °C or higher, there is no problem reading flash across the entire temperature range of -40 °C to 125 °C. This errata does not apply to –A (Automotive Grade) devices.

Impacts: Flash bits programmed at temperatures below 0 °C might not read back correctly at elevated temperatures.

Workaround: Program the flash in production and in-system at 0 °C or higher. If programming must be performed at temperatures lower than 0 °C, a validation of the flash at 25 °C or greater is highly recommended.

Resolution: Silicon Labs is continuing to investigate this issue. There is no resolution at this time.

3. **Description**: If the /RST pin is held low for more than 1 second while power is applied to the device, and then /RST is released, a percentage of devices may "lock up", and fail to execute code. Toggling the /RST pin does not clear the condition. The condition is cleared by cycling power. Most devices that are affected will show the lock up behavior only within a narrow range of temperatures (a 5 to 10 degrees C window).

   Impacts: Devices that lock up due to this issue will fail to execute code until the next power-on reset.

   Workaround: Ensure that the reset low time does not exceed 1 second.

   Resolution: Silicon Labs has identified a solution to this problem and this solution has been tested and qualified. Parts with the fix do not have any restrictions on /RST low time. The silicon revision remains the same, but Revision B parts that implement the fix can be identified visually using the assembly date code marking on the device. A four-digit assembly build date code is marked on each part on the bottom-most line. This is in the format YYWW, where YY is the two-digit assembly build calendar year and WW is the two-digit assembly build work week. All parts that have an assembly date code of 1124 or later (year 2011, work week 24) do not have any restrictions on /RST low time.

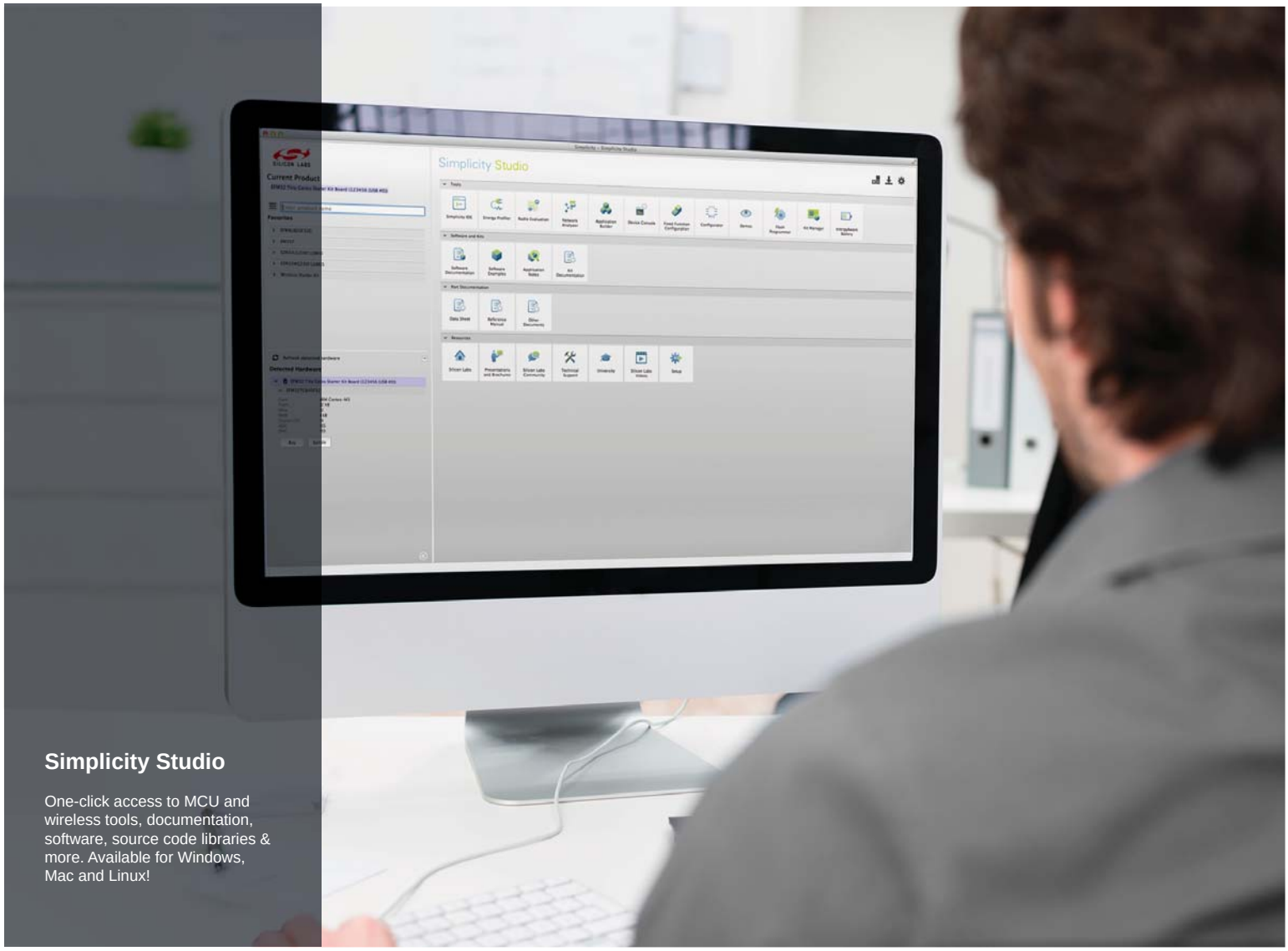
4. **Description**: The minimum limit of the V_{DD} Monitor (VDDMON0) low threshold can be slightly lower than the value specified in the datasheet. Table 2.7 "Reset Electrical Characteristics" of the datasheet (Rev 1.3) specifies $V_{RST-LOW}$ with a min–max range of 1.7 – 1.8 V. The updated range is 1.65 – 1.8 V.

   Impacts: None.

   Workaround: None.

   Resolution: The next revision of the datasheet (v1.4) will include the updated range for $V_{RST-LOW}$.

Note: C8051F5xx products are AEC-Q100 compliant and qualification and fault coverage reports are available upon request. A list of Silicon Laboratories sales representatives can be found at www.silabs.com. The next revision of the device datasheet will include this note in the relevant sections.



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